

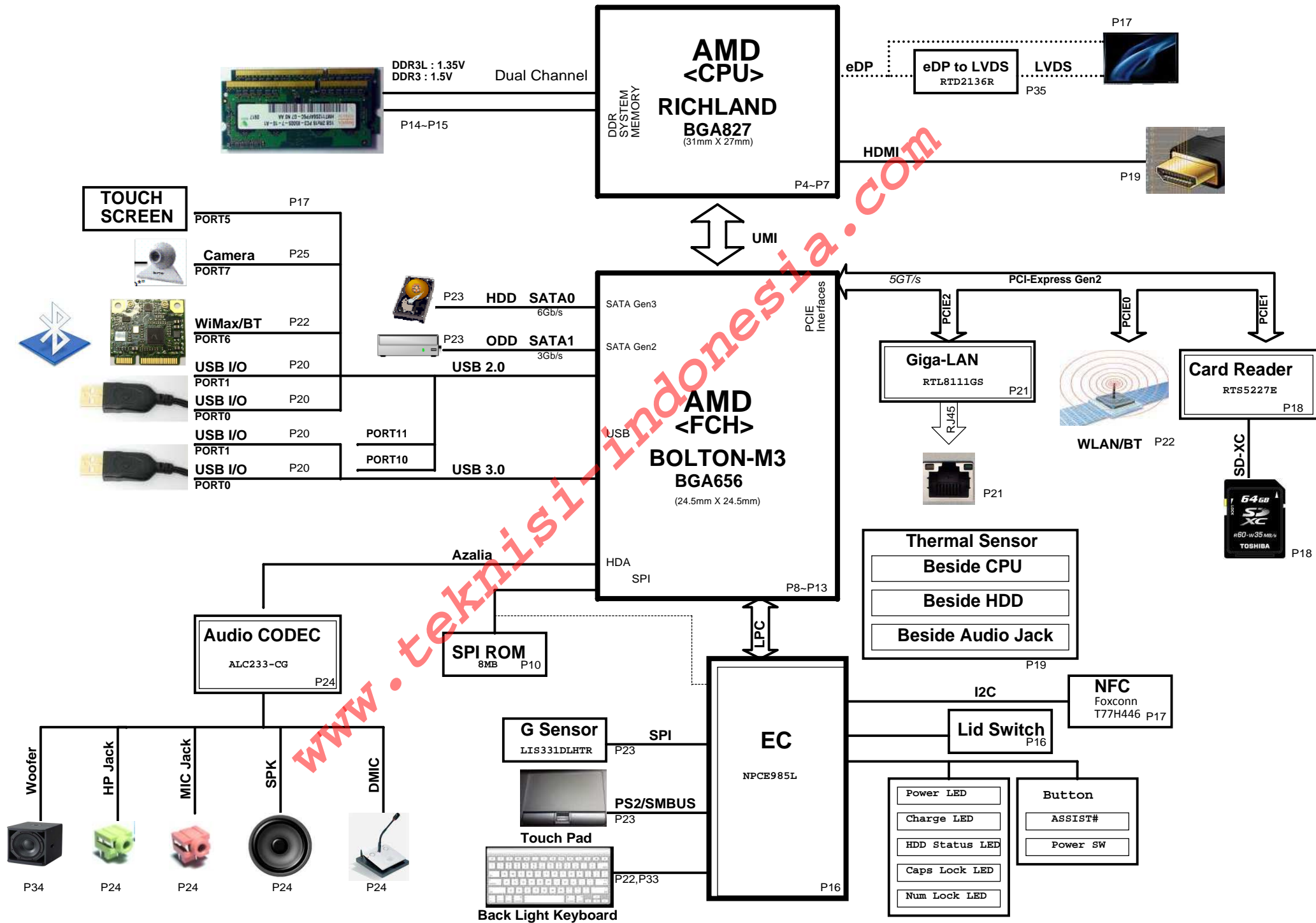
Page	Title of schematic page	Rev.	Date
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03	Change List	1A	
04	FP2 1/4(PEG&UMI)	1A	
05	FP2 2/4(DDR3 I/F)	1A	
06	FP2 3/4(DP/MISC)	1A	
07	FP2 4/4(POWER/GND)	1A	
08	FCH 1/6(GPIO/USB/AZ)	1A	
09	FCH 2/6(UMI/PCIE/PCI/CLK)	1A	
10	FCH 3/6(SATA/VGA/SPI)	1A	
11	FCH 4/6(POWER)	1A	
12	FCH 5/6(Strap)	1A	
13	FCH 6/6(GND)	1A	
14	DDR3 DIMM-0-STD	1A	
15	DDR3 DIMM-1-STD	1A	
16	WPCE985L & FLASH	1A	
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18	CARD READER(RTS5209)	1A	
19	HDMI/THERMAL	1A	
20	USB	1A	
21	LAN (RTL8111GS)	1A	
22	WLAN/KB-BL	1A	
23	HDD/ODD/G-SENSOR/TP/FAN	1A	
24	Audio ALC233-CG	1A	
25	LED/PS/DMIC\Camera	1A	
26	POWER +VCC_CORE (ISL62771)	1A	
27	POWER 3VPCU&RVCC5(TPS51427)	1A	
28	POWER 1.35VSUS/VTT_MEM	1A	
29	POWER +1.1V(G5602R41U)-5A	1A	
30	POWER VCC1.2/VCC2.5/Thermal	1A	
31	POWER(BAT IN / ADA IN/ UL)	1A	
32	POWER CHARGER (ISL88731C)	1A	
33	HOLE/EMI/KB	1A	
34	eDP to LVDS	1A	
35	IO PORT LIST	1A	

* : No mount
I@ : For native eDP output
D@ : For eDP to LVDS output

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HKA BLOCK DIAGRAM

02



Change List

MB_SCH_DVT_001
P21 Reserve U30,LR12,LR13,LC21
Reason : For LAN S5 wake up won't be supported.
Possible Risk: No.

MB_SCH_DVT_002
P25 Chang R198 and R309 resistor
Reason : Modify circuit for LED Light
Possible Risk: No.

MB_SCH_DVT_003
P22 Delete R333 0ohm and add F9(0.35A) fuse
P22 Delete R468[100K],Q33[2N7002]
Reason : Modify circuit for KB BL protection.
Possible Risk: No.

MB_SCH_DVT_004
P9 Change part of Crystal Y1 32.768K.
Reason : Original part is EOD.
Possible Risk: No.

MB_SCH_DVT_005
P8 Modify circuit for NFC function.
Change R865,R866 to R861,R864.
change NFC_EN from GPIO166 to GEVENT22#.
Reason : To enable NFC function.
Possible Risk: No.

MB_SCH_DVT_006
P16 Reserve diode KD4 for EC_PWRBTN#.
P22 Reserve diode D12 for WLAN_RF_ON.
Reason :For cost down.
Possible Risk: No.

MB_SCH_DVT_007
P20 Add choke for USB ports.
P25 Add choke for Camera USB interface.
Reason :EMI issue.
Possible Risk: No.

MB_SCH_DVT_008
P7,P11 Change capacitors 22U X5R 0805 to 22U X5R 0603.
Reason :To enlarge the distance between Cap. and Keyboard.
Possible Risk: No.

MB_SCH_DVT_009
P33 Change FCH NUT shape.
Reason :To fit screw's size.
Possible Risk: No.

MB_SCH_DVT_010
P16 Add KR42 10K ohm.
Reason :To fit LVDS panel power sequence.
Possible Risk: No.

MB_SCH_DVT_011
P8 Add SMBUS path from FCH to RTD2136R.
Reason :Reserve the way to flash RTD2136R eFuse.
Possible Risk: No.

MB_SCH_DVT_012
P9,P21 Change Capacitors for XTAL Y2, LY1.
Reason :For more precisely frequency of XTAL.
Possible Risk: No.

MB_SCH_DVT_013
P19 Change Resistor of HDMI signals resistors.
Reason :For better HDMI signal quality.
Possible Risk: No.

POWER

2A-P1
Change PC580 and PC599 from 0.047u to 0.068 for fine tune IC response

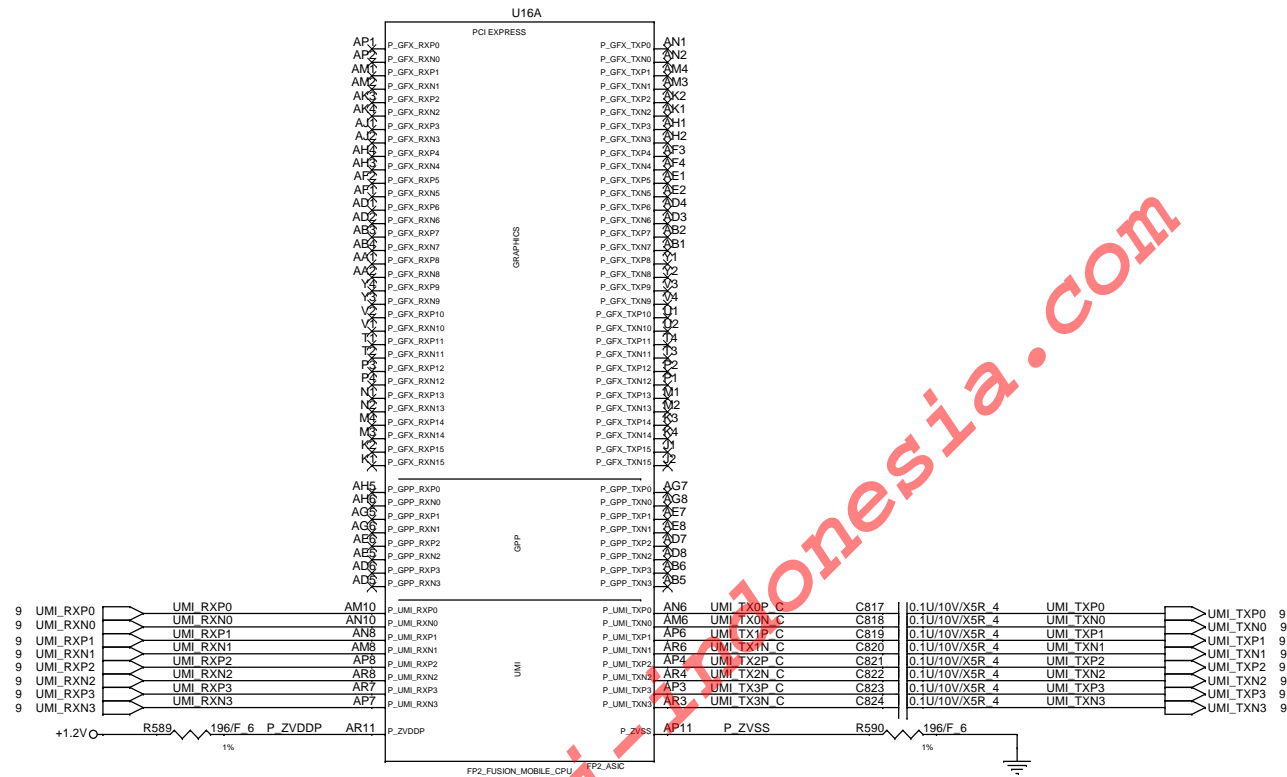
2A-P2
add PC617, PC618, PC619, PC620 for meet AMD SPEC of ripple

2A-P3
change PR58 from 255k to 196k for fine tune OCP

2A-P4
change from 3.75k to 3K for fine tune OCP

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1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



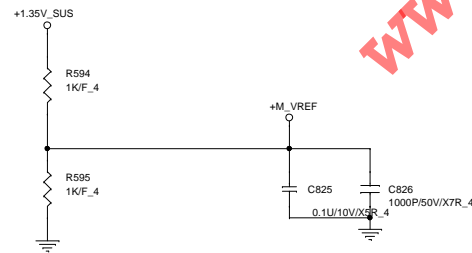
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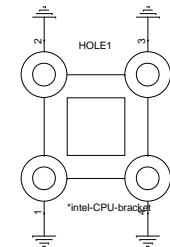
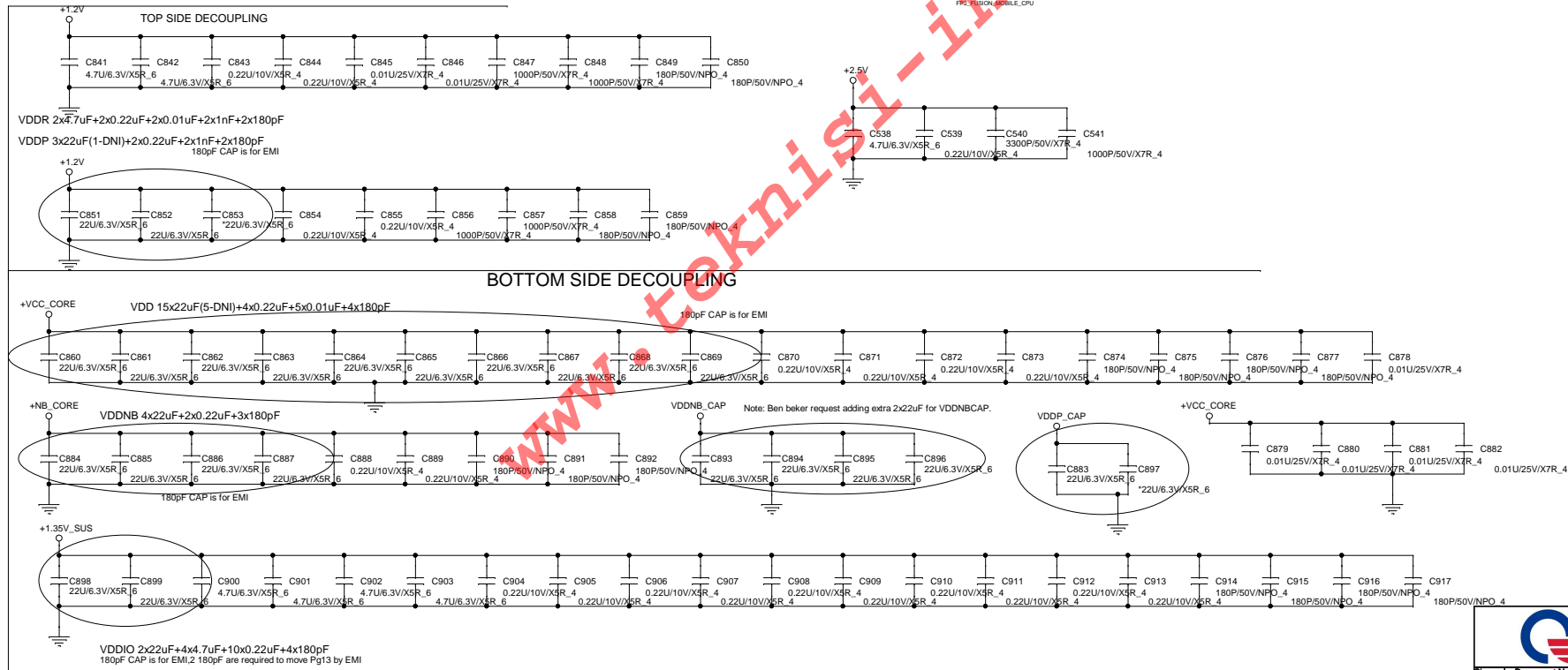
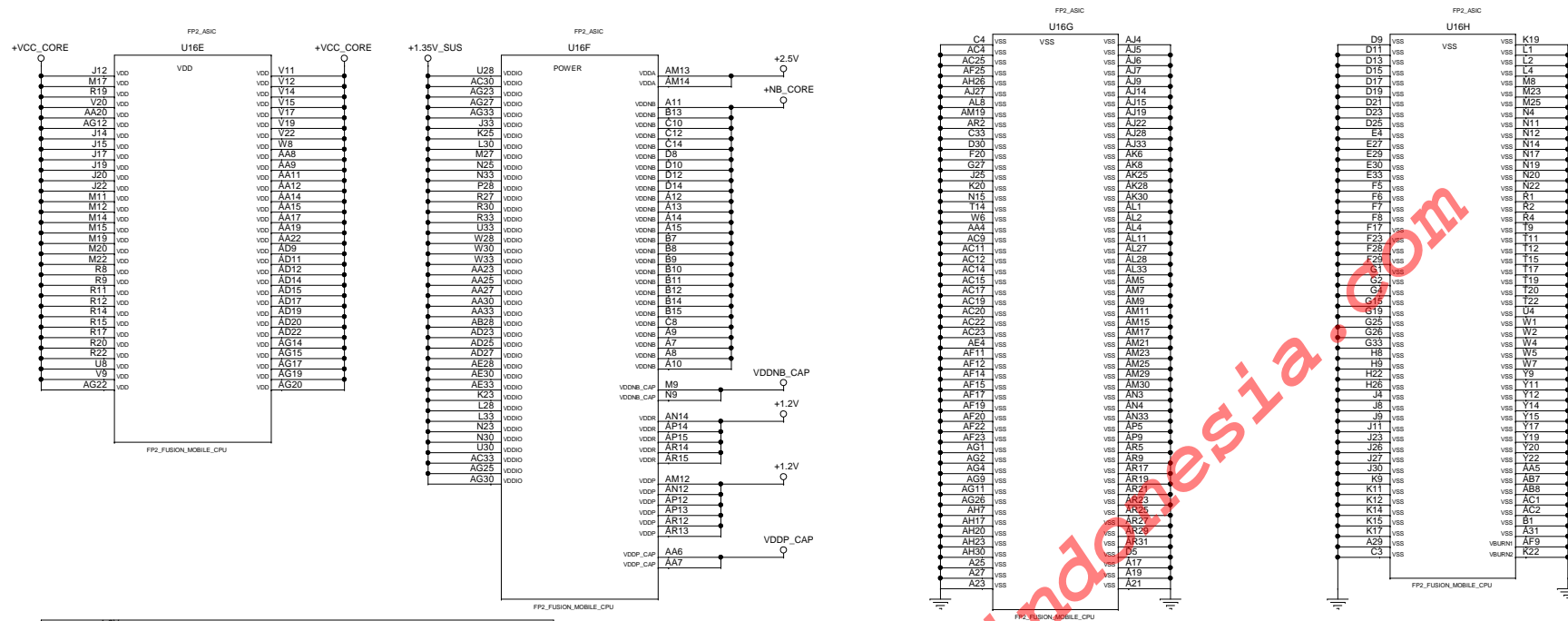
PROJECT : HKB

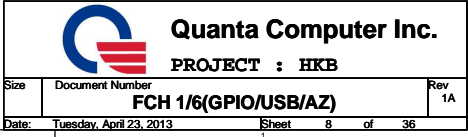
FP2 1/4(PEG&UMI)

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1	1	1A
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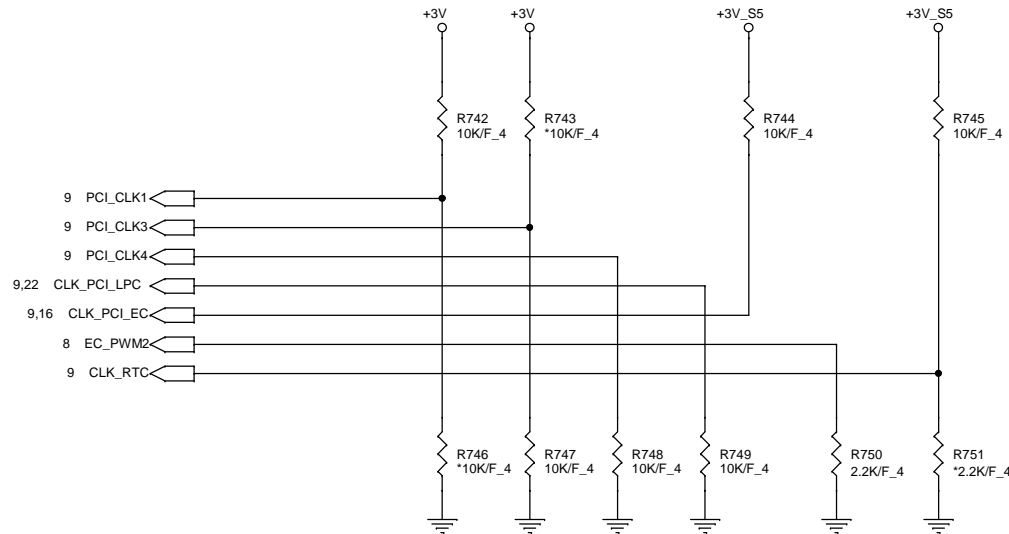




STRAPS PINS



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.



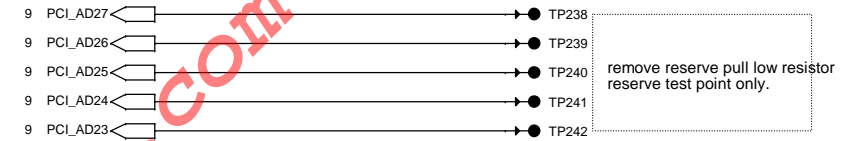
REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	(LPCCLK0) CLK_PCI_LPC	(LPCCLK1) CLK_PCI_EC	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	Reserved	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	Required setting for integrated clock mode DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE enable

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DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



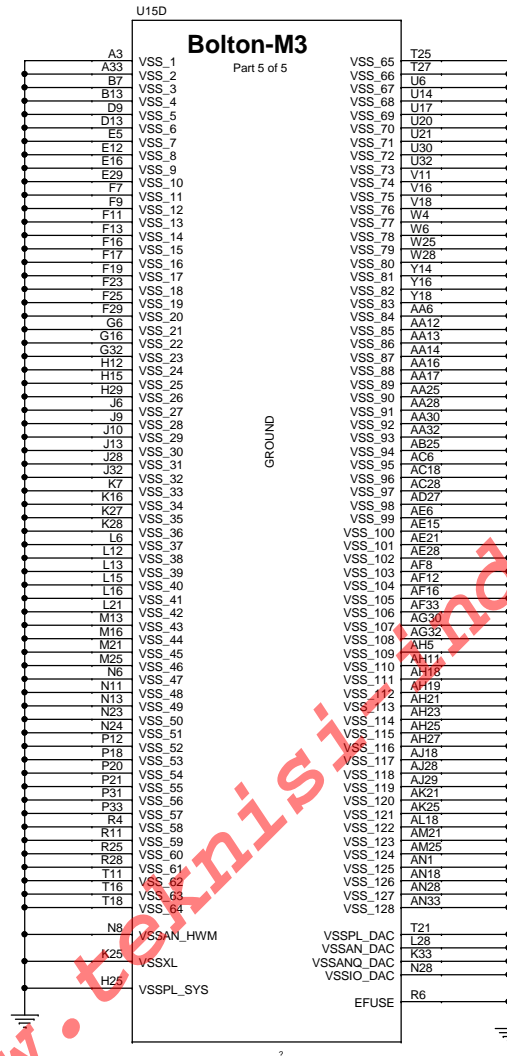
	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT		normal REFCLK DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL		Inverted REFCLK	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



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	FCH 5/6(Strap)	1A
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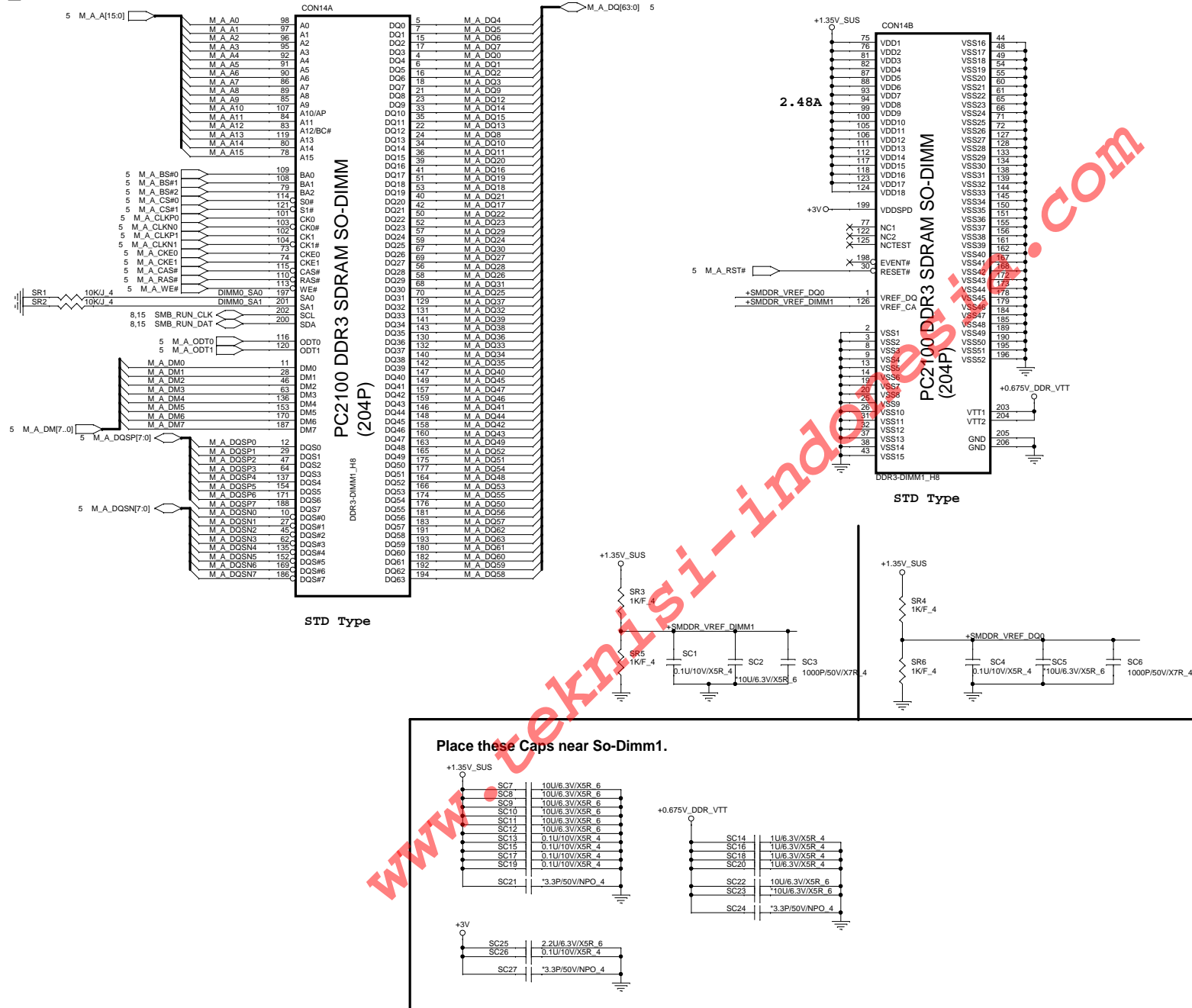
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PROJECT : HKB

Size	Document Number	Rev
		1A
FCH 6/6(GND)		
Date:	Tuesday, April 23, 2013	Sheet 13 of 36

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

DDR_RVS (DDR)

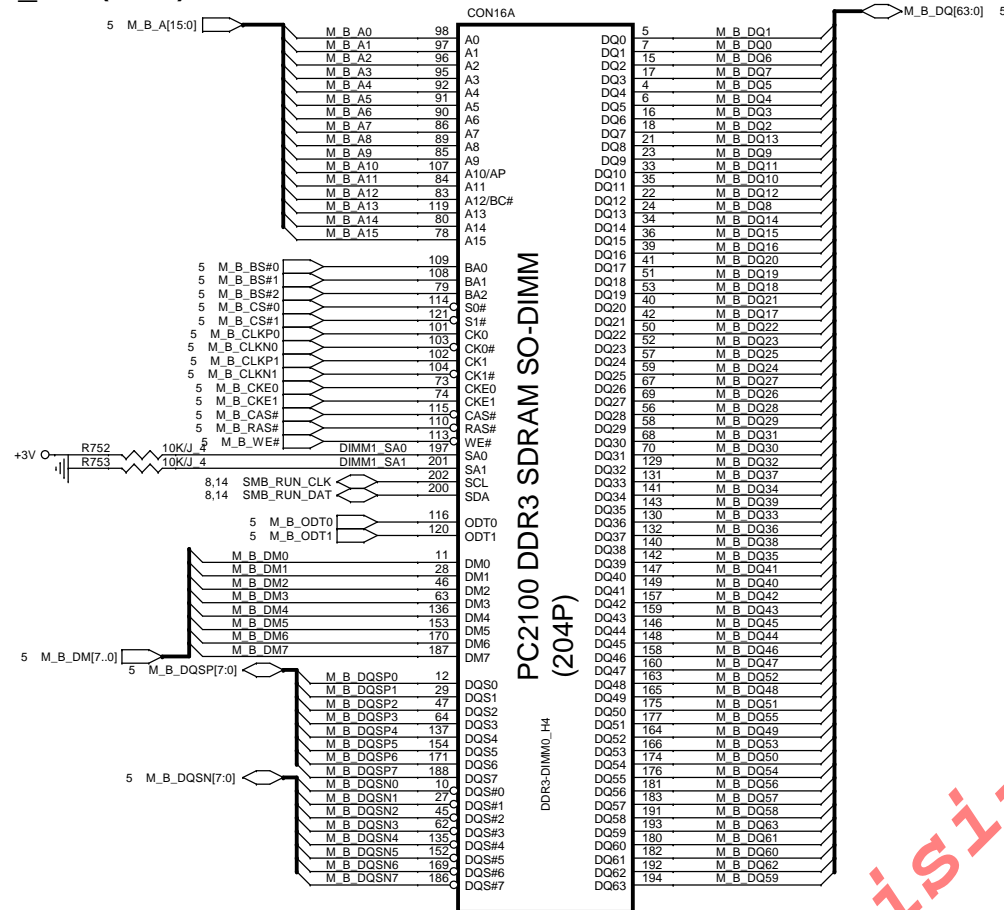


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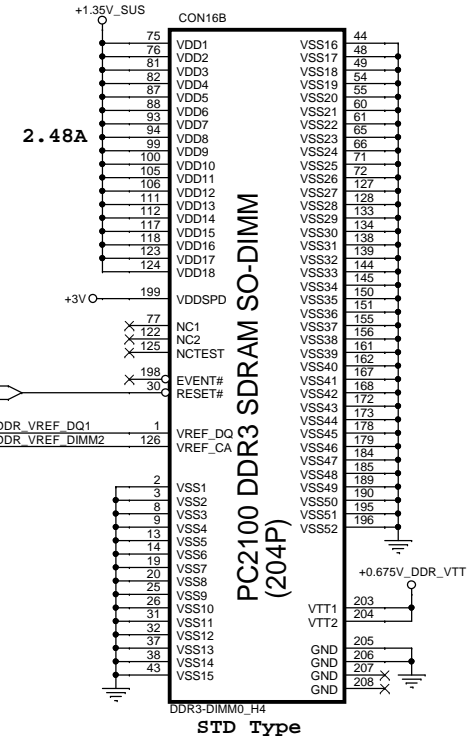
PROJECT : HKB

Date	Document Number	Rev
Tuesday, April 23, 2013	DDR3 SO-DIMM-0	1A
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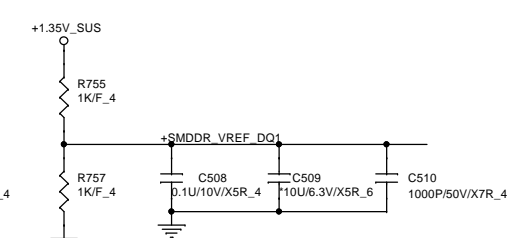
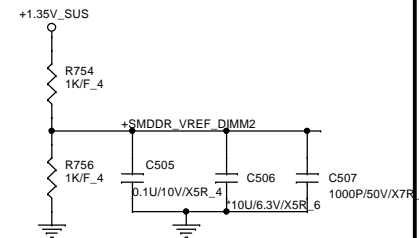
DDR_STD (DDR)



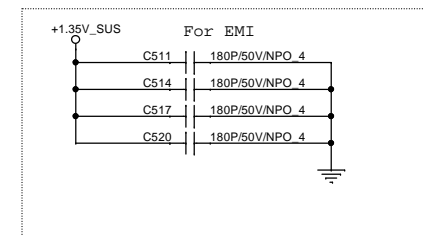
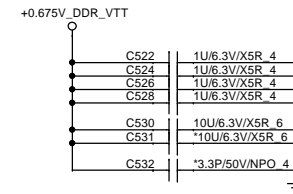
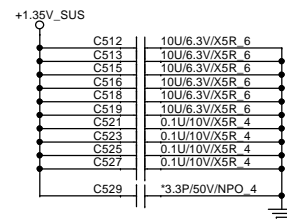
STD Type



STD Type



Place these Caps near So-Dimm1.



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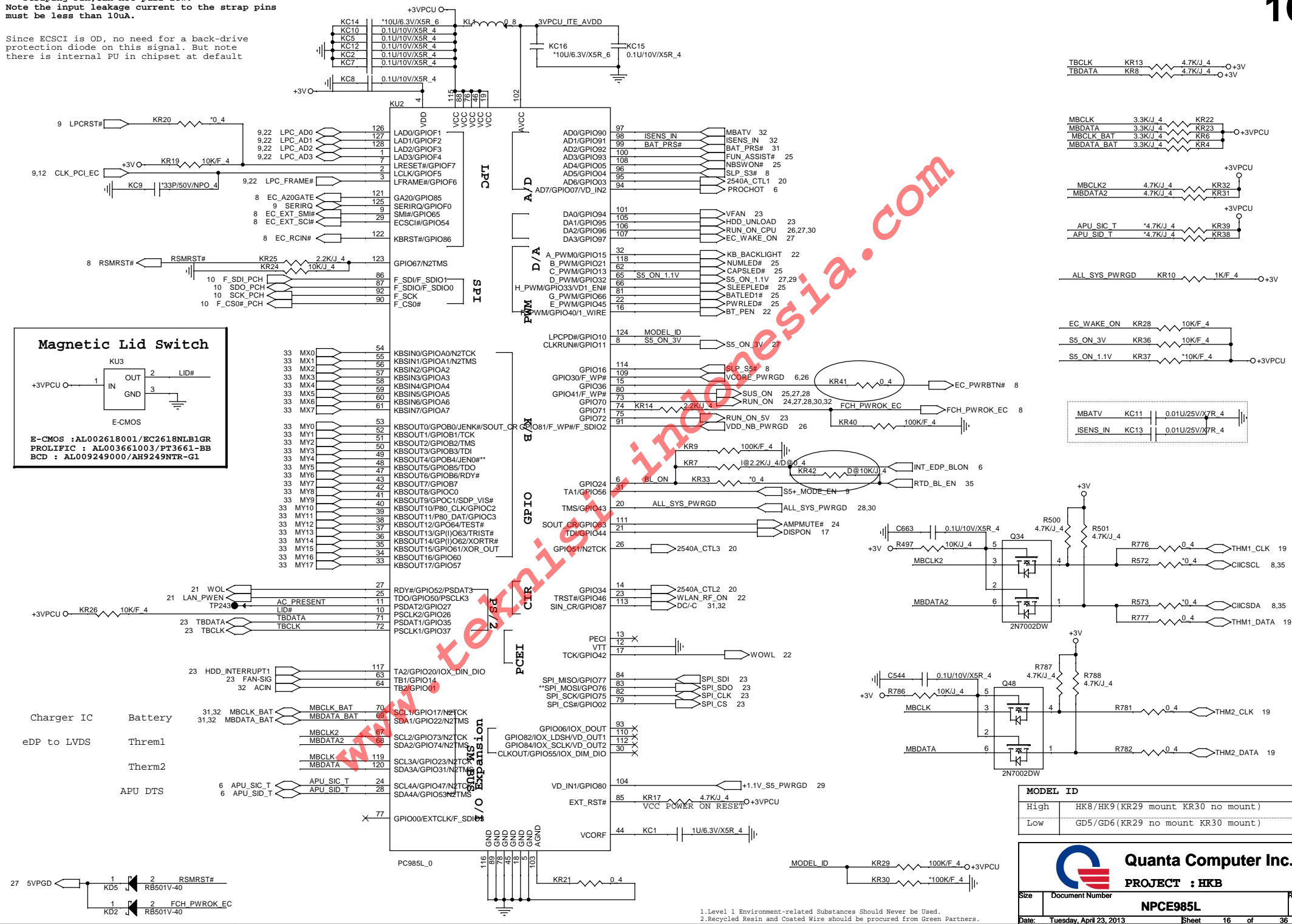
DDRIII SO-DIMM-1

Size	Document Number	Rev
		1A
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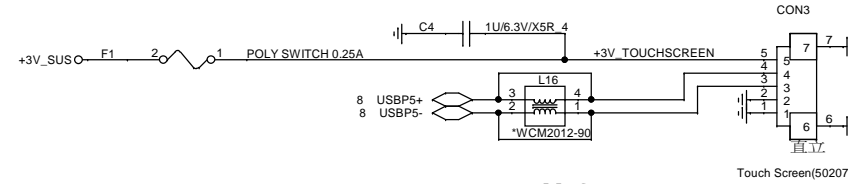
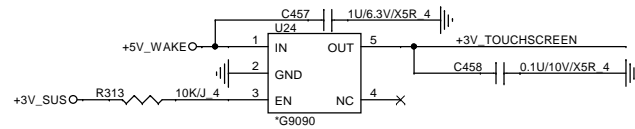
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

** Strapping Pin, Can not pull low.
Note the input leakage current to the strap pins
must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



Touch Screen



Add for EMI

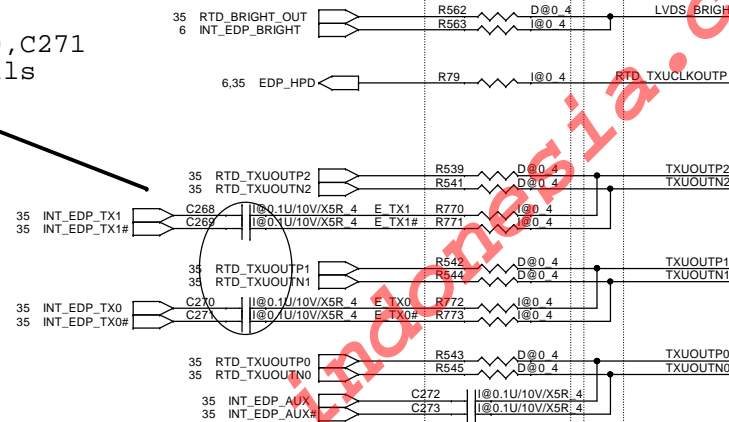
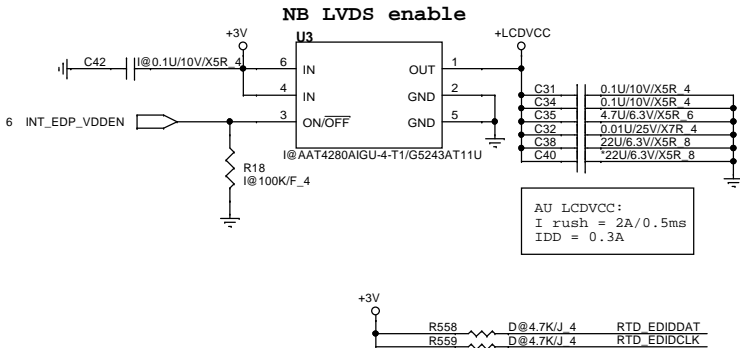
Camera HD specification
Voltage: Max. 3.6V
Current: Max. 200mA
OCP: 200mA - 300mA

Distance between C268,C269,C270,C271
and CON5 must larger than 500 mils

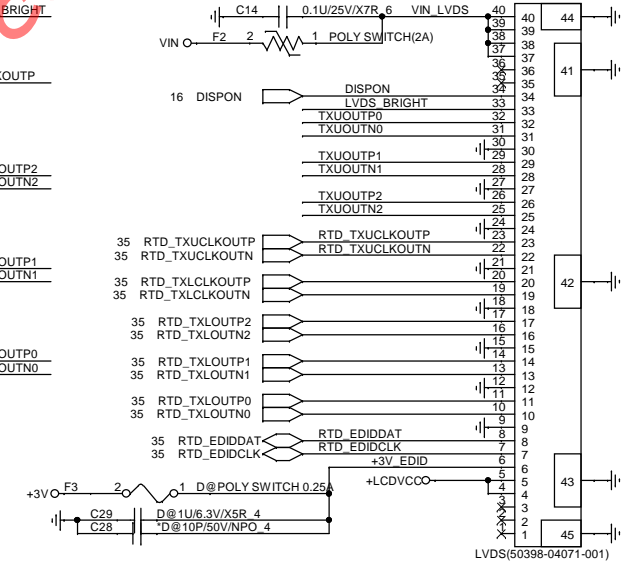
Close to connector

FAST, UL/CSA

LVDS



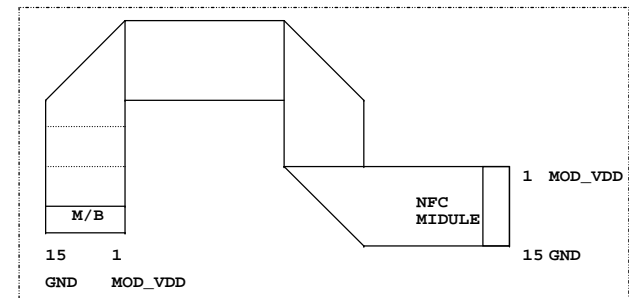
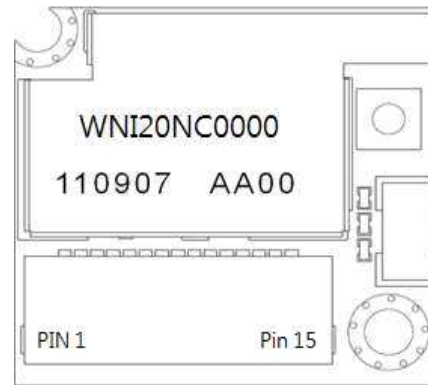
Branches are as short as possible!!



For EMI.
Close to CON20

NFC_DETECT#	C813	*10P/50V/COG 4
NFC-IRQ	C814	*10P/50V/COG 4
SMB_NFC_CLK	C815	*10P/50V/COG 4
SMB_NFC_DAT	C816	*10P/50V/COG 4

NFC

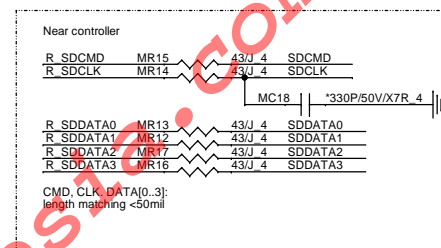


NFC module :
Vender : Samsung SNC-i20
Power consumption : Max. 160mW/48mA
Power Ripple +/- 50mV



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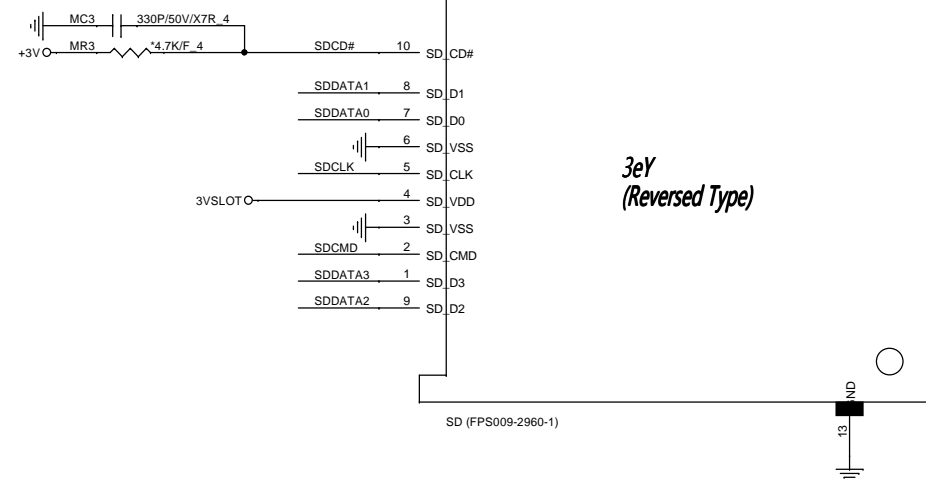
40 mil

MC7 0.1U/10V/X5R 4

MC4 1U/6.3V/X5R 4

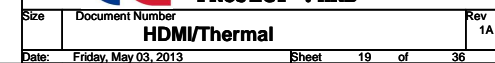
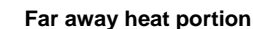
MC6 1U/6.3V/X5R 4

O-3V SLOT

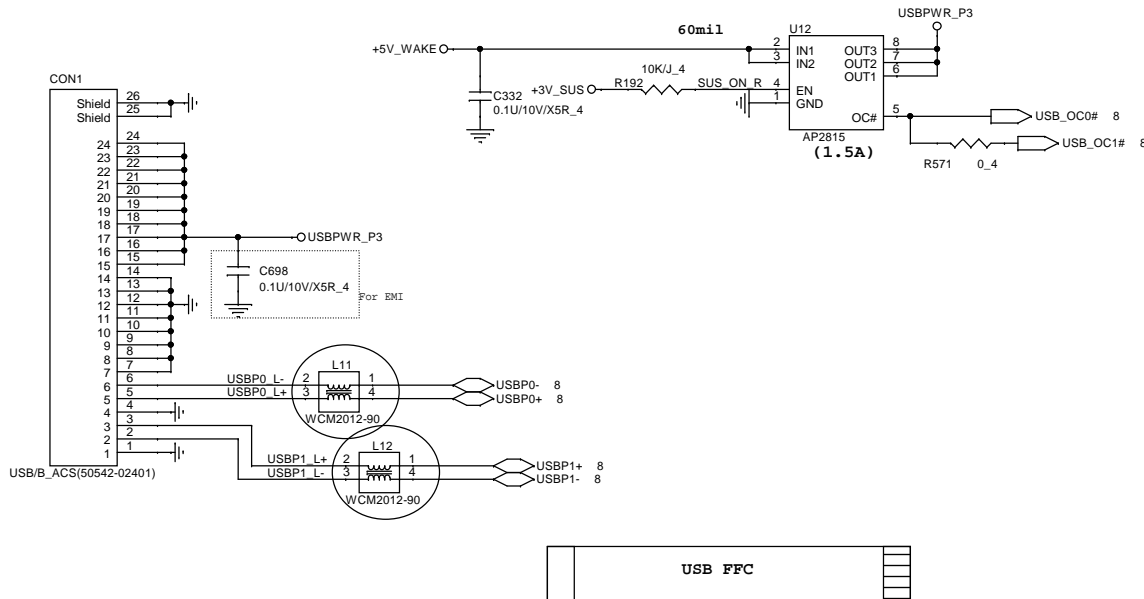




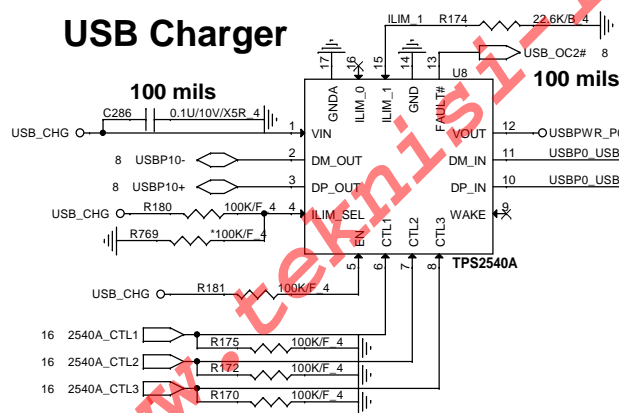
Close to FIN



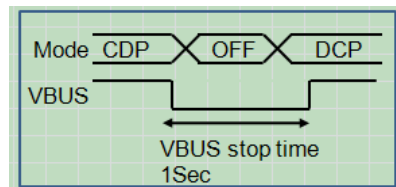
MB to USB board



USB Charger



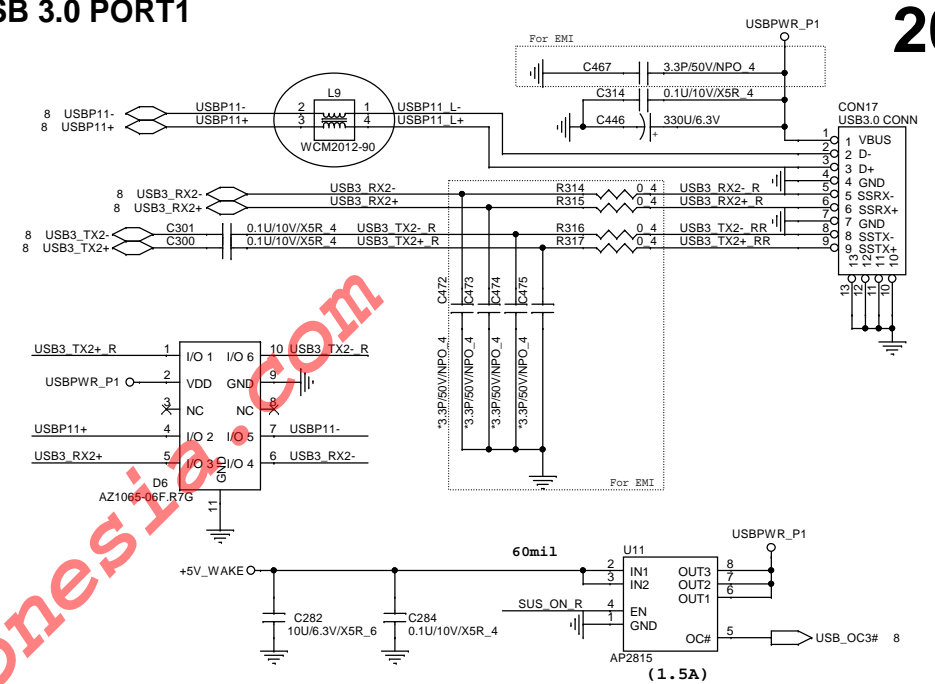
SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



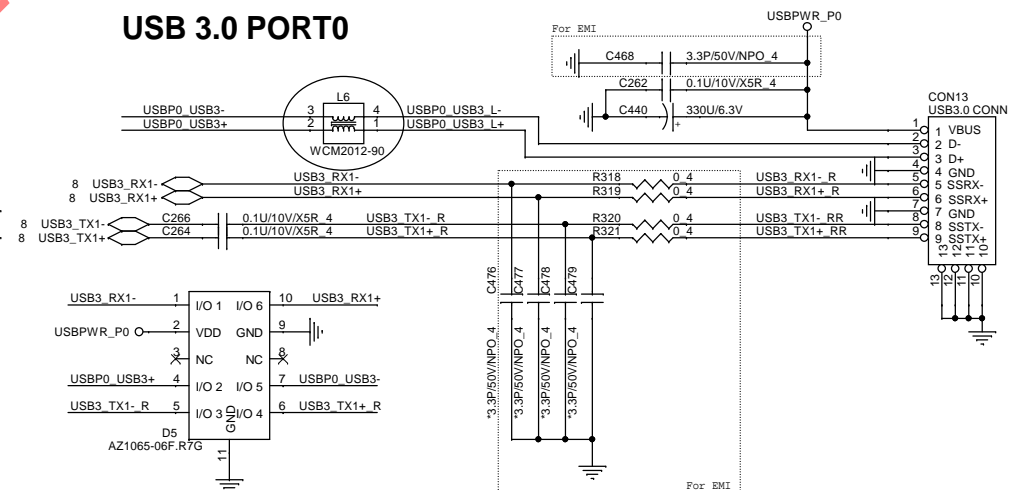
CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP, Auto-detect (S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode (S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only (S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only (S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

USB 3.0 PORT1



USB 3.0 PORT0



ILIM_SEL (I LIMIT(A)= 48000/R)		
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

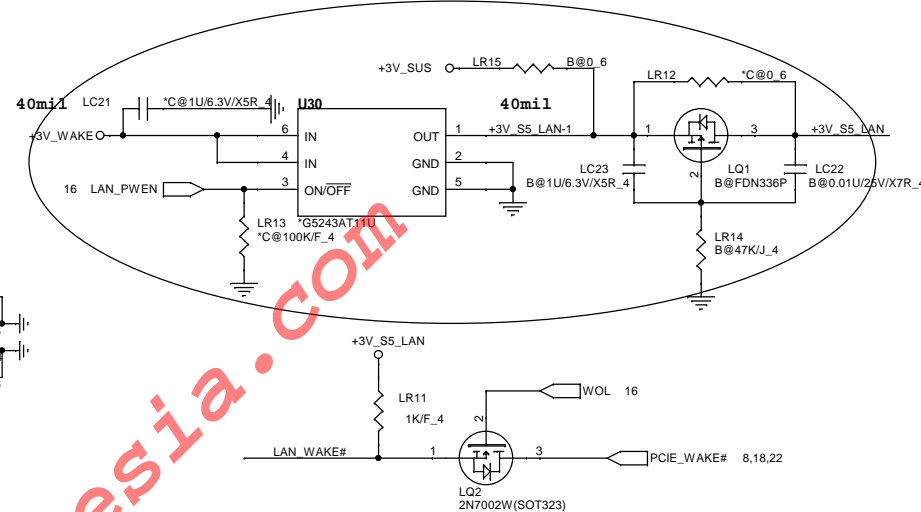


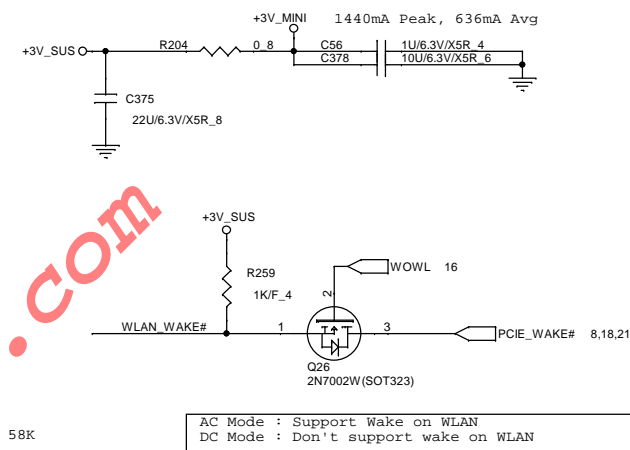
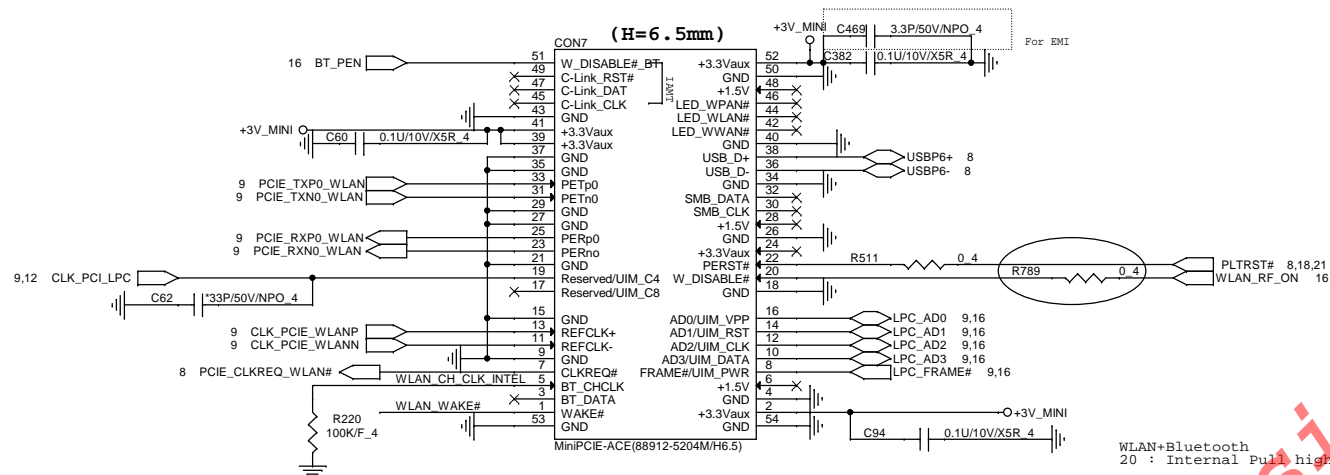
Diagram showing the pin connections for the RJ45 AOP(C100CE-10806-L) connector. The connector is labeled CON10 and has 10 pins. The connections are as follows:

MDI Label	Pin
MDI TXP0 TR	1
MDI TXN0 TR	2
MDI TXP1 TR	3
MDI TXP2 TR	4
MDI TXN2 TR	5
MDI TXN1 TR	6
MDI TXP3 TR	7
MDI TXN3 TR	8

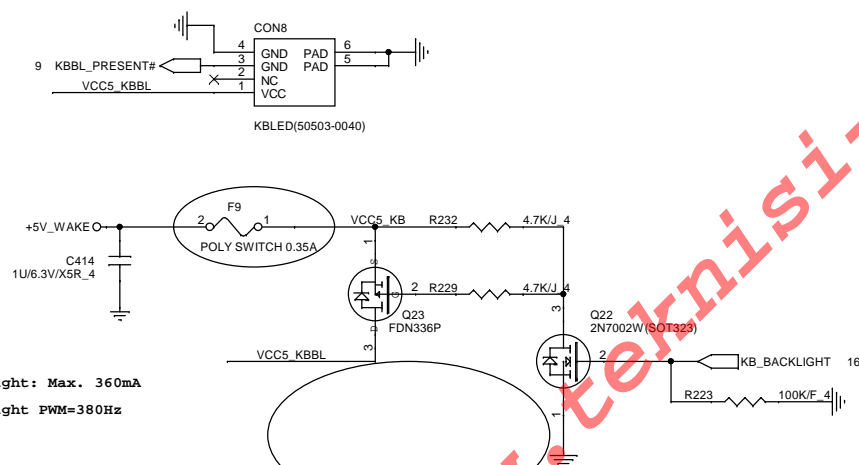
Pins 9 and 10 are shown as unconnected.

RJ45 AOP(C100CE-10806-L)

WLAN/WIMAX/WIDI



KB BACKLIGHT



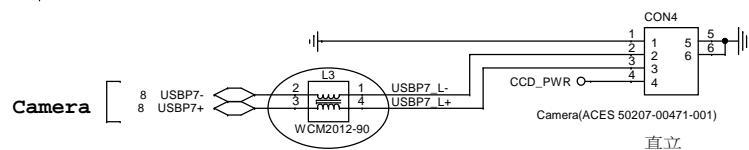
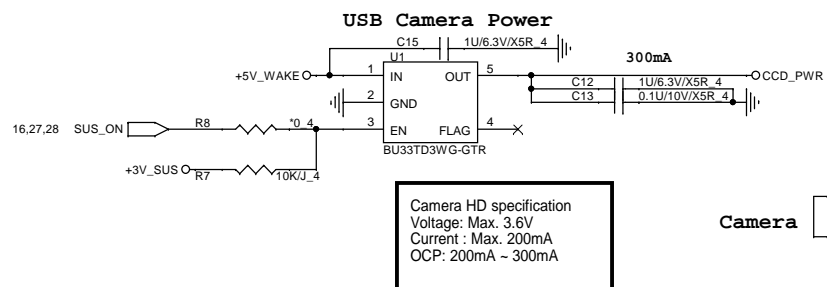
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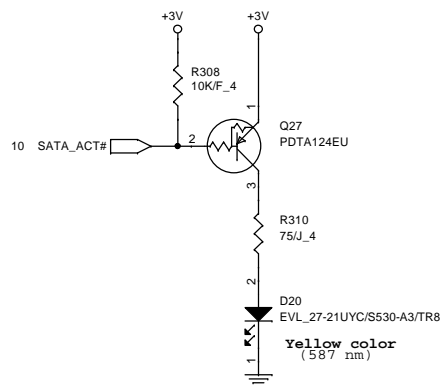
Size	Document Number	Rev
	WLAN/KB-BL	1A
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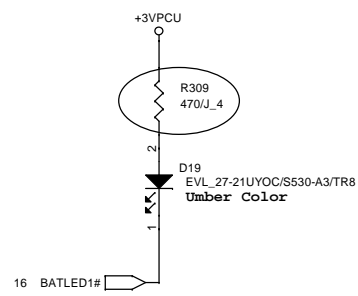
Camera



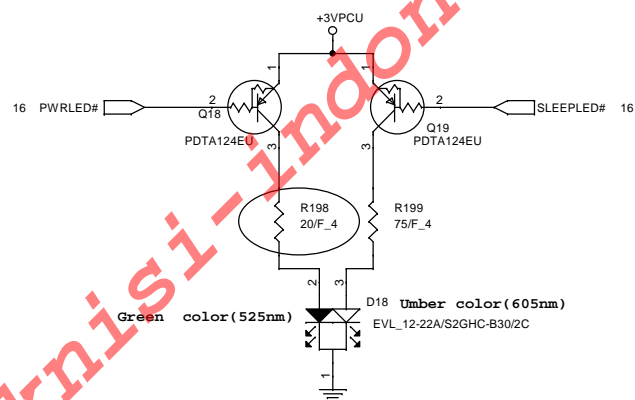
SATA LED



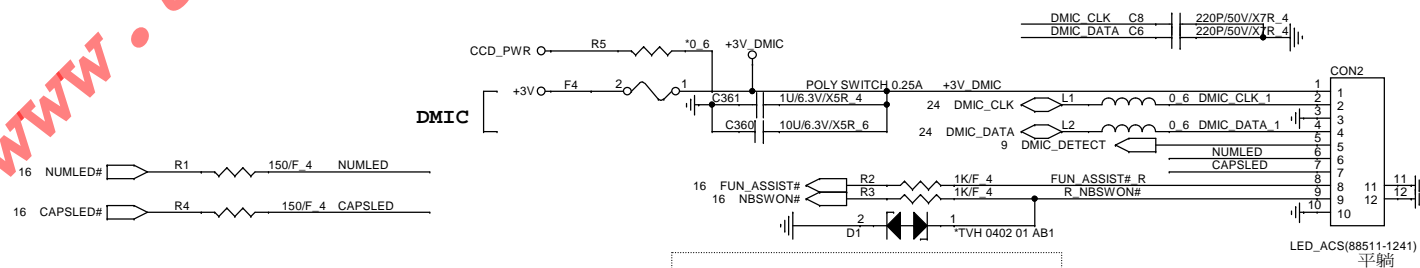
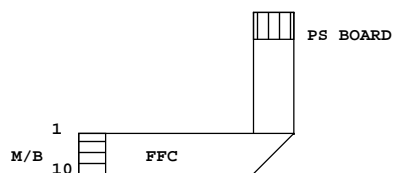
BATTERY LED



Power/Sleep LED



Power SW Board Connector



For EMI

CAPSLED	C364	*0.1U/10V/X5R 4
R NBSWON#	C366	*0.1U/10V/X5R 4
FUN ASSIST# R	C365	*0.1U/10V/X5R 4

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PROJECT : HKB

Size	Document Number
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Document Number

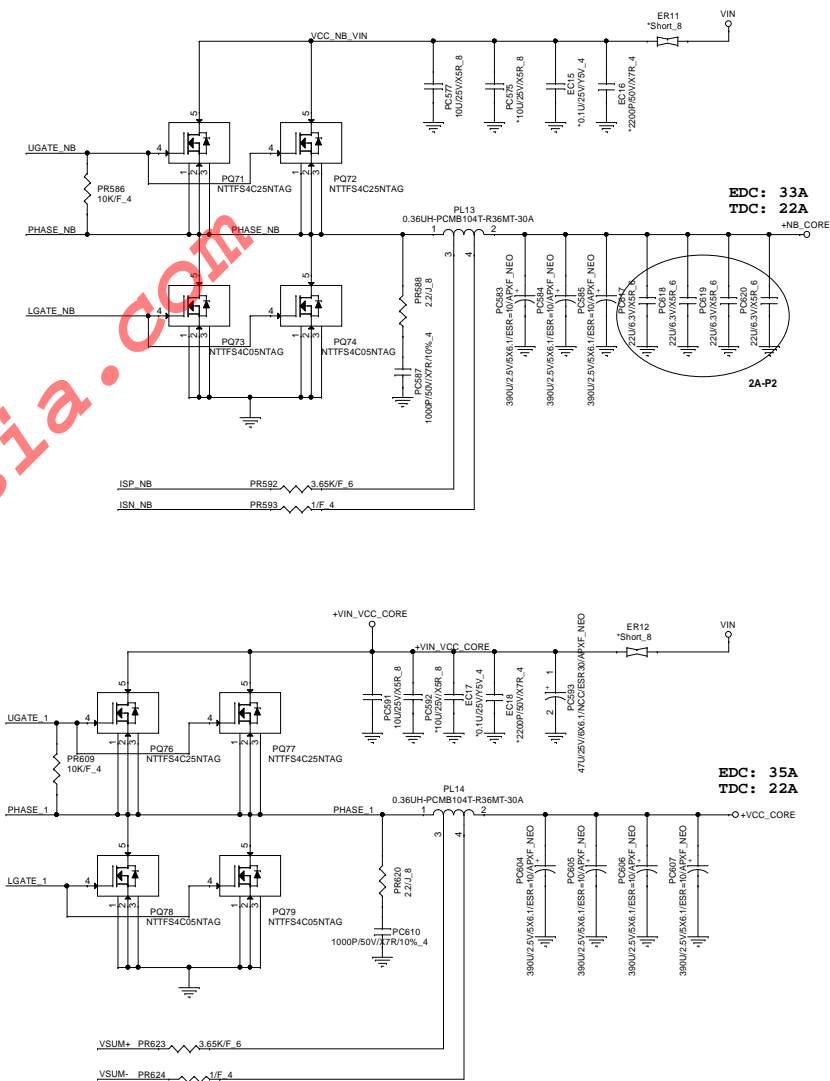
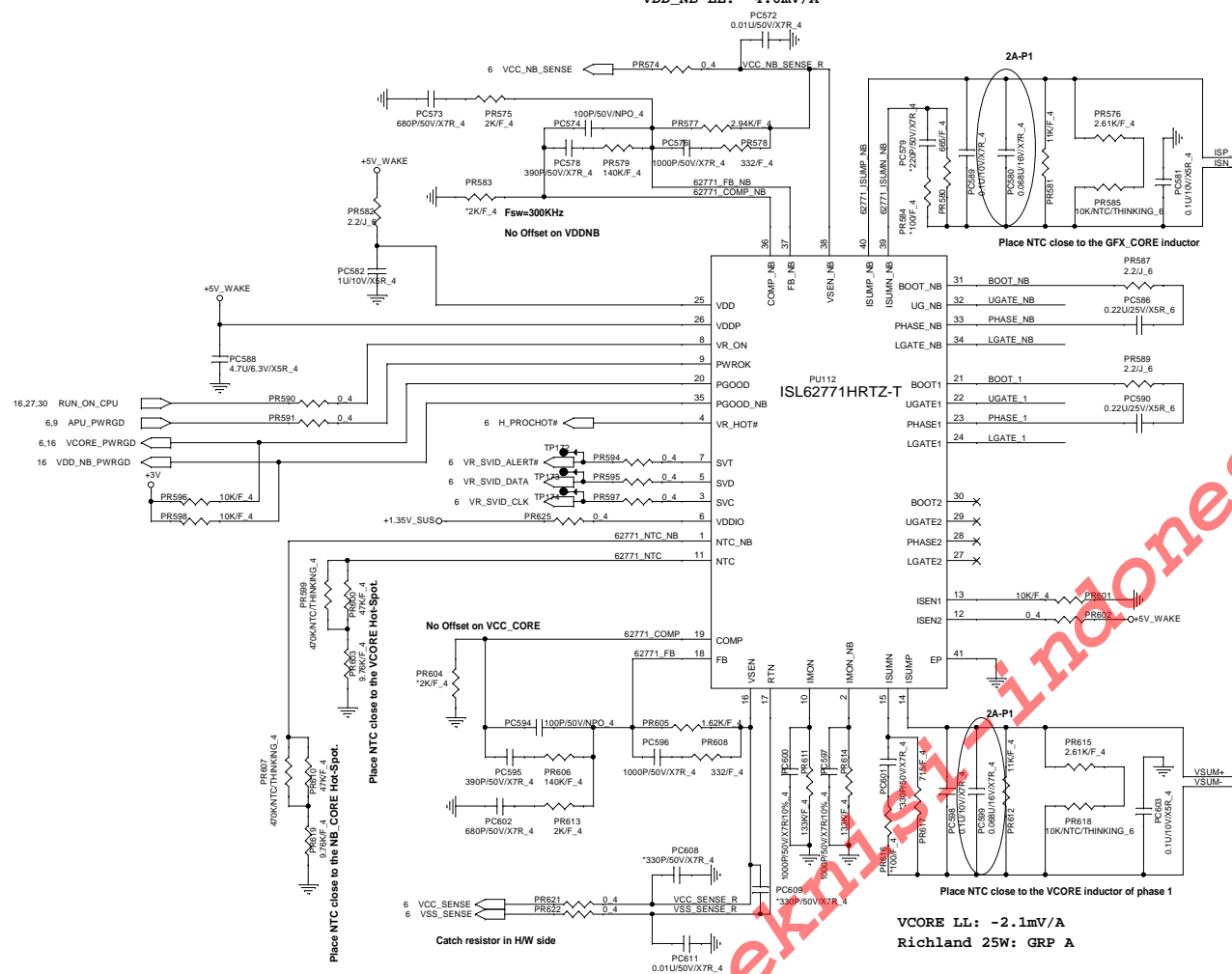
LED/PS/DMIC\Camera

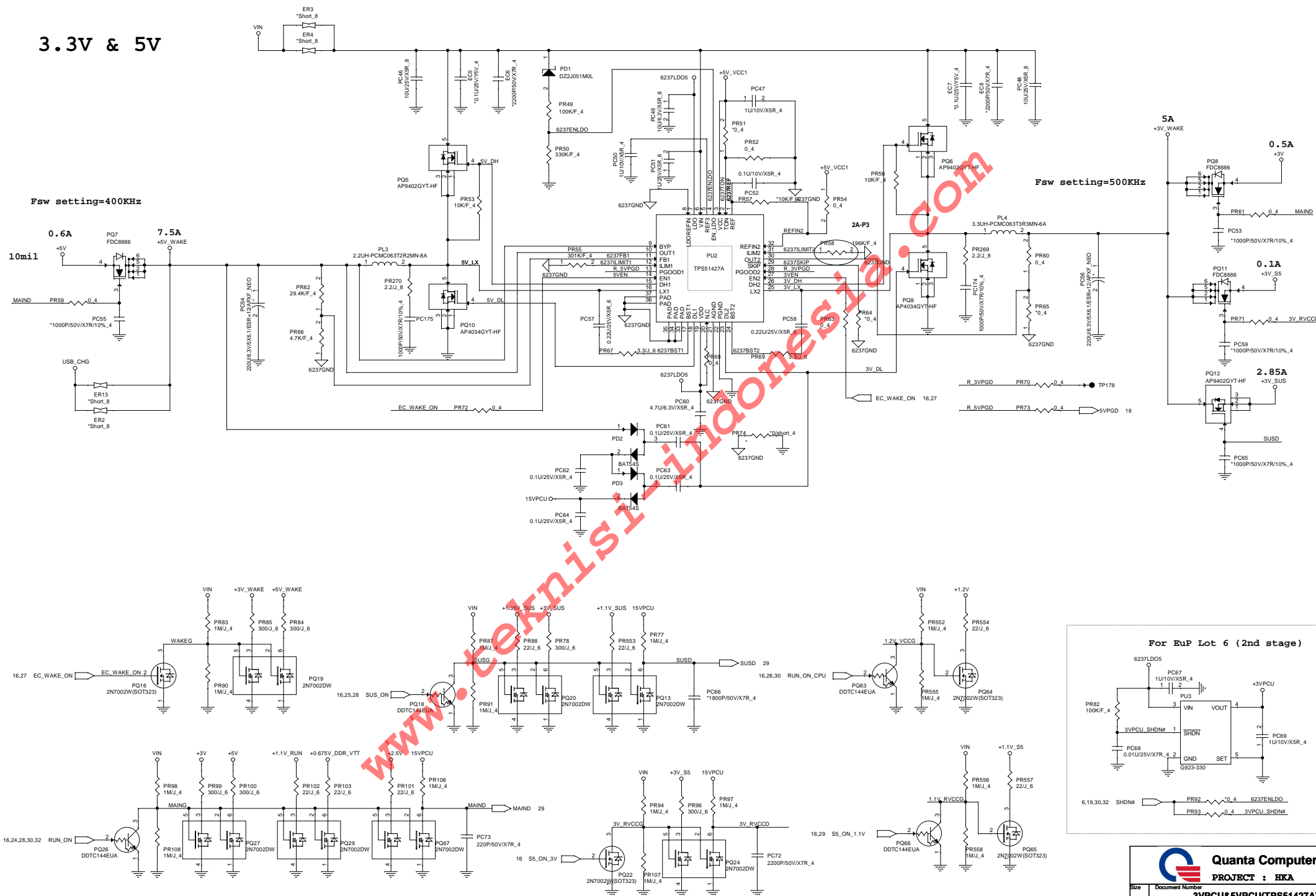
Date: Tuesday, April 23, 2013

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- 1.Level 1 Environment-related Substances Should Never be Used.
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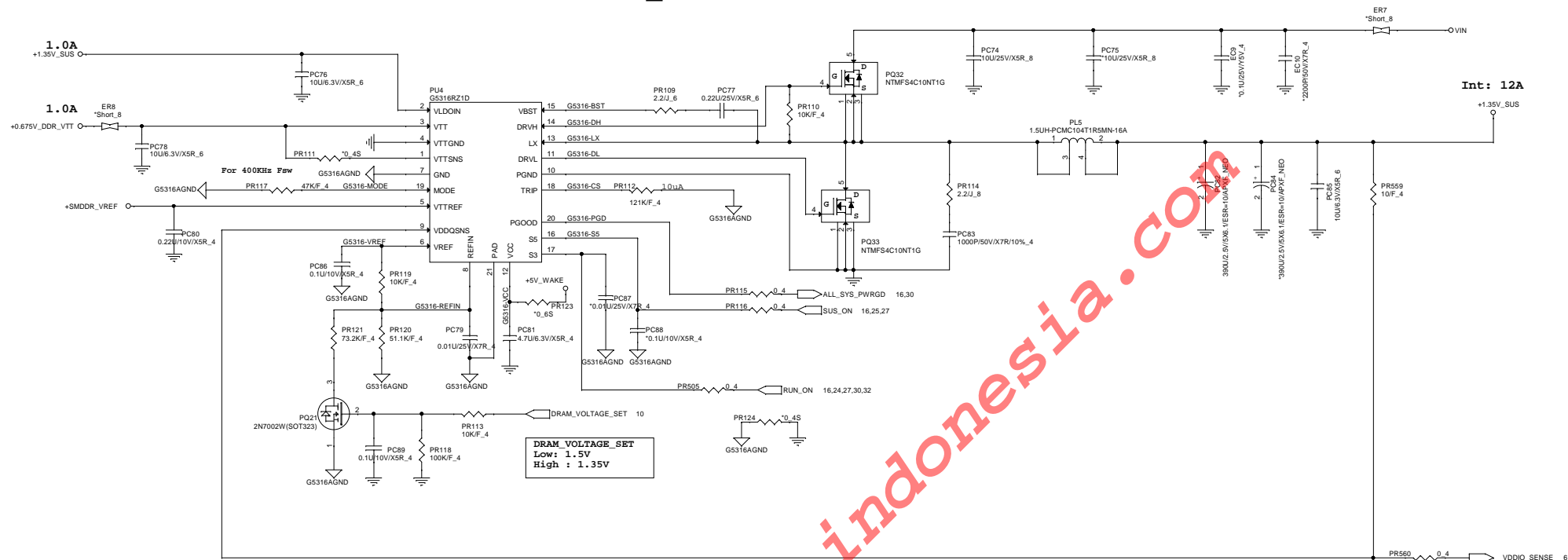
Richland 25W: GRP A
VDD_NB LL: -4.0mV/A





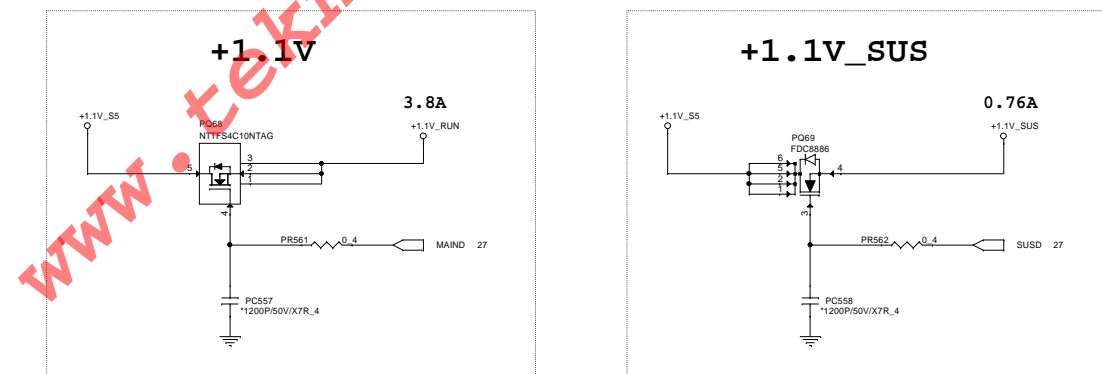
- 1.Level 1 Environment-related Substances Should Never be Used.
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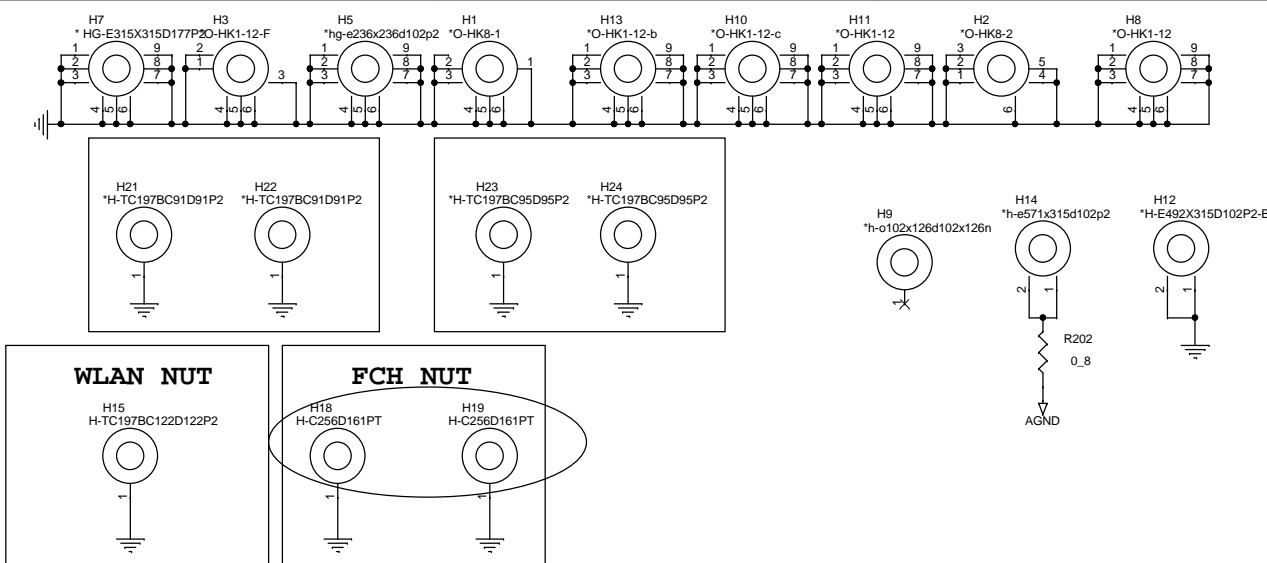
1.35VSUS & VTT_MEM



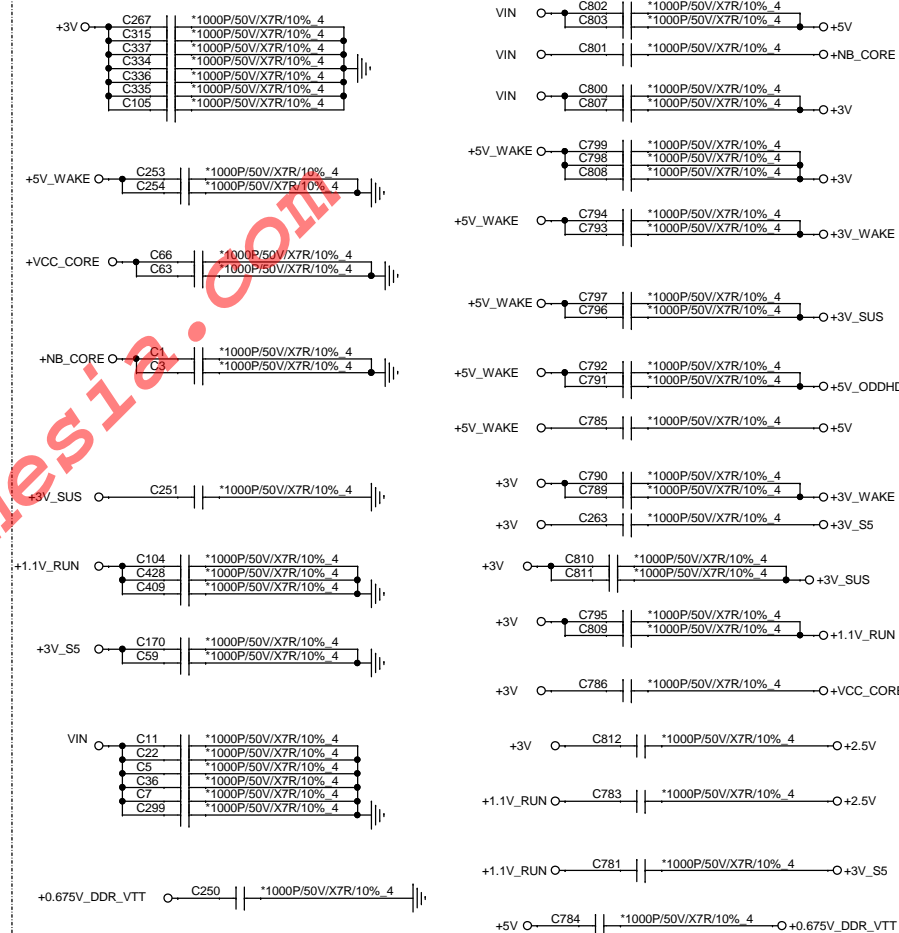
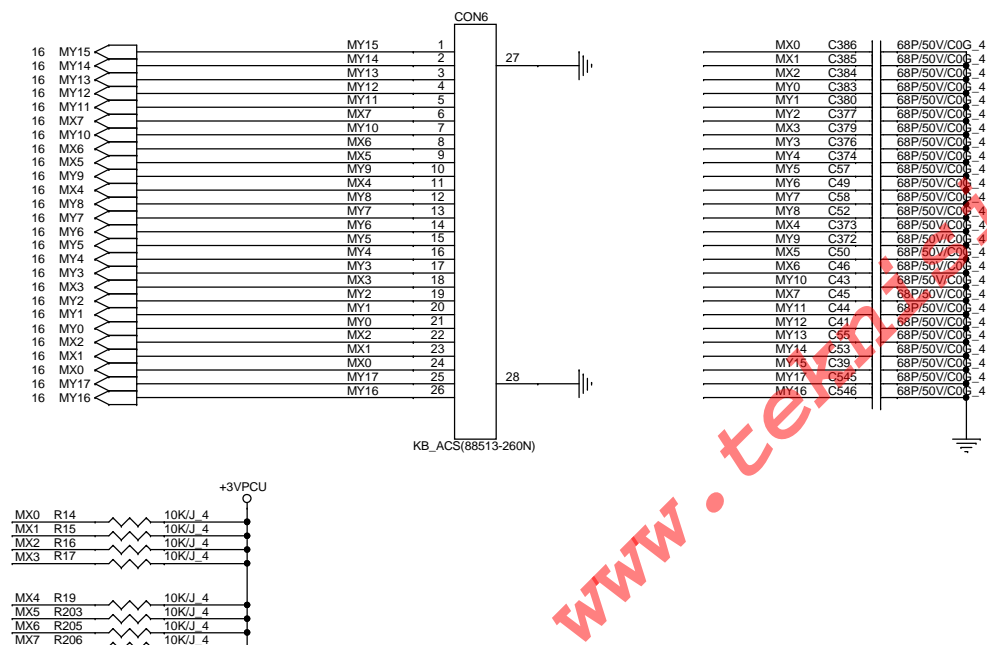
MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



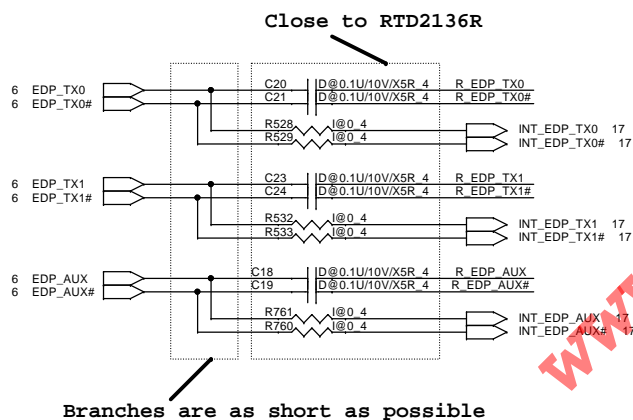
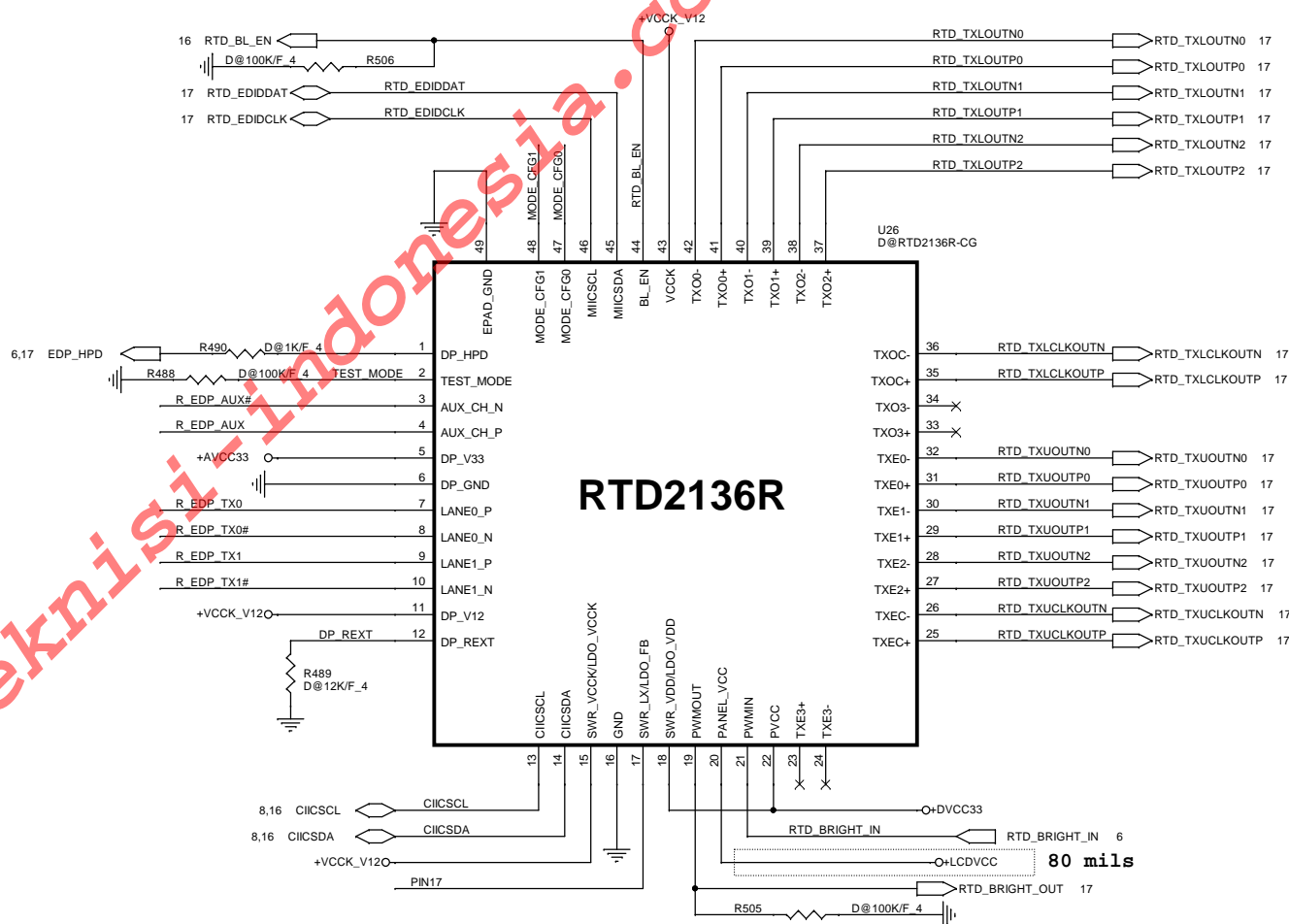
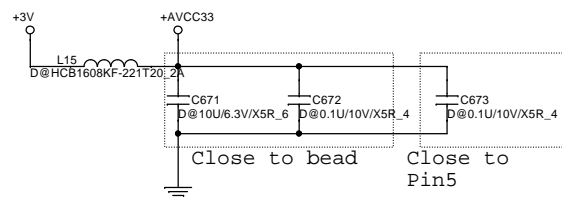
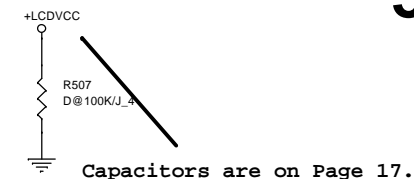
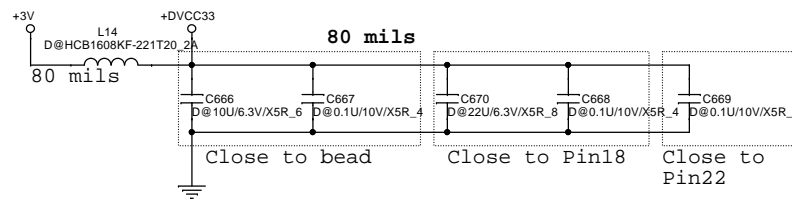
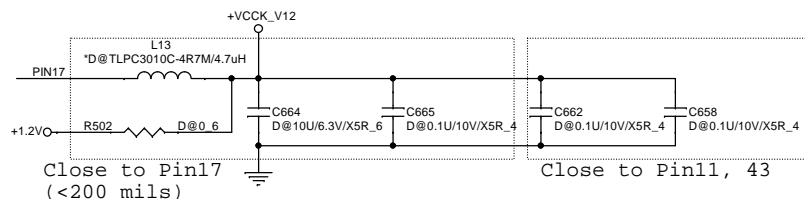


KEY BOARD Connector



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

1. Level 1 Environment-related Substances Should Never be Used.
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eDP to LVDS

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I/O PORT LIST

USB PORT Architecture	
PORT 0	USB2.0
PORT 1	USB2.0
PORT 2	N/A
PORT 3	N/A
PORT 4	N/A
PORT 5	Touch Screen
PORT 6	WiMAX/BT
PORT 7	Camera
PORT 8	N/A
PORT 9	N/A
PORT 10	USB3.0
PORT 11	USB3.0
PORT 12	N/A
PORT 13	N/A

PCIE BUS	
PORT 0	WLAN Port
PORT 1	CARD READER
PORT 2	GLAN(RTL8111GS)
PORT 3	N/A

SATA BUS	
PORT 0	HDD
PORT 1	ODD
PORT 2	N/A
PORT 3	N/A
PORT 4	N/A
PORT 5	N/A

M/B ID LIST

SIZE	Board ID0
HKA 14"	0
HKB 15"	1

I/F	Board ID1
eDP	0
LVDS	1

CPU	Board ID2	Board ID3
A4	0	0
A6	0	1
A8	1	0
A10	1	1

SM BUS LIST

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88732HRTZ-T	0001 001X	0001 0010	0001 0011	Charger

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS35A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB0_RUN_CLK/SMB0_RUN_DAT	WRITE	READ	Function
DIMM Module 0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII

SM BUS	SMB1_RUN_CLK/SMB1_RUN_DAT	WRITE	READ	Function
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

POWER MAP

	S0	S3	S4	S5 (Charger Enable)	S5 (Charger Disable)
RUN_ON_CPU	H	L	L	L	L
+NB_CORE	H	L	L	L	L
+VCC_CORE	H	L	L	L	L
+1.2V	H	L	L	L	L
RUN_ON	H	L	L	L	L
+5V	H	L	L	L	L
+3V	H	L	L	L	L
+2.5V	H	L	L	L	L
+1.1V_RUN	H	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L
SUS_ON	H	H	L	L	L
+1.35V_SUS	H	H	L	L	L
+3V_SUS	H	H	L	L	L
+1.1V_SUS	H	H	L	L	L
S5_ON_1.1V	H	H	*H/L	L	L
+1.1V_S5	H	H	*H/L	L	L
S5_ON_3V	H	H	*H/L	L	L
+3V_S5	H	H	*H/L	L	L
EC_WAKE_ON	H	H	*H/L	H	L
+3V_WAKE	H	H	*H/L	H	L
+5V_WAKE	H	H	*H/L	H	L
RUN_ON_5V	H	L	L	L	L
+5V_ODDHDD	H	L	L	L	L

* H: If wake up event exists.